# Naveed Ul Mustafa

## Education

Fall 2012– to date — **PhD in "Computer Engineering"**, *Bilkent University*, Ankara, Turkey, *3.42/4.0 CGPA*.
I am interested in areas of Computer Architecture, Network on Chip, Embedded Systems and Real Time Operating System. Currently I am working in area of reconfigurable MPSoC.

2009–2011 — **M.Sc in "System on Chip Design"**, *Royal Institute of Technology (KTH)*, Stockholm, Sweden, *3.0/4.0 CGPA*.

2003–2006 — **B.Sc in "Computer Engineering"**, *University of Engineering and Technology*, Taxila, Pakistan, *78.89 %*.

## Trainings

**OSE Basics:** A 3 day course by Laszlo Breznovits in Enea headoffice, Kista, Stockholm, Sweden.

**The Next Big Little Thing:** Hands-on Practice with the Internet of Things using Intel Edison Development Kit at ASPLOS 2015, Istanbul

## Experience

### Teaching

2007–2009 — **Lecturer**, *National University-Foundation for Advancement of Sciences and Technology*, Islamabad, Pakistan.
I served as Lecturer in Electrical Engineering Department of NU-FAST. I conducted labs and theory courses of

1. Microprocessor and Interfacing
2. Computer Organization and Architecture
3. Digital Communication
4. Analog Communication
5. Signals and Systems

### Internship at National Defense Complex, Islamabad, Pakistan

Sep 2006-Nov 2006 — *Design of Computer Based Exam Checking Application*

area — Digital Image Processing

tools employed — MATLAB

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## Master thesis

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|---|---|
| title | *Enriching Enea OSE for Better Predictability Support* |
| resources employed | Optima by ENEA, ENEA OSE, C++ programming, MS Visio, Latex |
| examiner | Dr. Ingo Sander, Royal Institute of Technology (KTH), Stockholm, Sweden |
| supervisor | Mehrdad Saadatmand, Industrial PhD Scholar at Mälardalen University (MDH), Sweden |
| area | Real Time Operating Systems |
| abstract | A real-time application is designed as a set of tasks with specific timing attributes and constraints. These tasks can be categorized as periodic, sporadic or aperiodic, based on the timing attributes that are specified for them which in turn define their runtime behaviors. To ensure correct execution and behavior of the task set at runtime, the scheduler of the underlying operating system should take into account the type of each task (i.e., periodic, sporadic, aperiodic). This is important so that the scheduler can schedule the task set in a predictable way and be able to allocate CPU time to each task appropriately in order for them to achieve their timing constraints.<br><br>ENEA OSE is a real-time operating system with fixed priority preemptive scheduling policy which is used heavily in embedded systems, such as telecommunication systems developed by Ericsson. While OSE allows for specification of priority levels for tasks and schedules them accordingly, it can not distinguish between different types of tasks.<br><br>This thesis work investigates mechanisms to build a scheduler on top of OSE, which can identify three types of real-time tasks and schedule them in a more predictable way. The scheduler can also monitor behavior of task set at run-time and invoke violation handlers if time constraints of a task are violated.<br><br>The scheduler is implemented on OSE5.5 soft kernel. It identifies periodic, aperiodic and sporadic tasks. Sporadic and aperiodic tasks can be interrupt driven or program driven. The scheduler implements EDF and RMS as scheduling policy of periodic tasks. Sporadic and aperiodic tasks can be scheduled using polling server or background scheme.<br><br>Schedules generated by the scheduler deviate from expected timing behavior due to scheduling overhead. Approaches to reduce deviation are suggested as future extension of thesis work. Usability of the scheduler can be increased by extending the scheduler to support other scheduling algorithms in addition to RMS and EDF. |

## KTH design project in M.Sc.

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| title | *Design and Implementation of Probe Based Serial and Parallel Search Algorithm for Network on Chip (NoC)* |
| HDL used in project | VHDL |
| tools employed | Modelsim, Design Compiler & MATLAB |
| examiner | Dr. Axel Jantsch, KTH, Stockholm, Sweden |
| supervisor | Dr. Meganathan, KTH, Stockholm, Sweden |

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| area | Digital Design |
| description | In this project, a serial search algorithm for establishing connection between two nodes on a NoC is implemented using VHDL. Another parallel search algorithm is proposed and designed. Minute implementation details for both algorithms are finalized. Simulation is performed using Modelsim. Efficiency parameters in both cases are measured and compared. |

## Final year degree project in B.Sc.

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| title | *Implementation of MC-CDMA modem on ADSP BF 561* |
| supervisor | Dr. Muid Mufti, MD Telematix Corporation, Blue area, Islamabad, Pakistan |
| tools employed | MATLAB, C/C++ |
| DSP employed | ADSP BF 561 |
| area | Digital Signal Processing |

## Languages

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| English | **Advance** | *Fluent in writing and speaking* |
| Urdu | **Advance** | *Fluent in writing and speaking* |
| Punjabi | **Advance** | *Fluent in speaking* |
| Turkish | **Intermediate Level** | |

## Qualification Exams

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| IELTS | **Academic** | *7.5/9.0* |
| GRE | **General** | *305/340* |

## Computer skills

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| programming | Assembly language of 8051 microcontroller and 8084 & 8086 microprocessors, C, C++, Java | languages for embedded systems | Ada 2005 |
| system level modeling | SystemC, TLM using SystemC | hardware descriptive languages | VHDL, Verilog |
| simulation and modeling tools | MATLAB, UML, Noxim, gem5, ESESC | technical softwares/tools | NIOS II IDE, Quartus 9.0, SoPC, Cadence Design Tool, Microwind, Verologger Pro, Pspice, Modelsim, Xilinx ISE, Code Composer Studio, AutoCAD, Keil $\mu$ vision, Visio, LaTeX |
| engineering kits | NIOS II IDE Board for Cyclone FPGA, Xilinx FPGA Kit, ADSP BF 561 EZ Lite Kit by Analog Devices, DSP Starter Kit for the TMS320C6713 | OS for embedded systems | MicroC/OS II,OSE: Real-Time Operating System from ENEA |

operating systems: MS Windows 9x,2000&XP, Linux

## Areas of interest

Network on Chip

System on Chip Architecture

Digital Design and FPGA

Embedded Systems and Software

Real Time Operating Systems

## Publications

*Adaptive Routing Framework for Network on Chip Architectures*: Accepted for inclusion in the ASPLOS ACM SRC 2015, Istanbul, Turkey.

*Monitoring Capabilities of Schedulers in Model-Driven Development of Real-Time Systems*: Published in 17th IEEE International Conference on Emerging Technologies & Factory Automation (ETFA 2012),Krakow, Poland.

*Concept and Design of Exhaustive-Parallel search algorithm to support Quality-of-service in Network-on-Chip*: Published in 24th IEEE International SOC Conference (SOCC 2011), Taipei, Taiwan.

M.Sc. thesis report: *Enriching Enea OSE for Better Predictability Support.* To view thesis report, please follow the link `http://kth.diva-portal.org/smash/record.jsf?searchId=1&pid=diva2:438101`

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## References

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